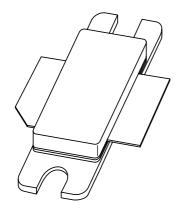
DISCRETE SEMICONDUCTORS

DATA SHEET



BLL1214-250L-band radar LDMOS transistor

Product specification Supersedes data of 2002 Feb 05 2002 Aug 06





L-band radar LDMOS transistor

BLL1214-250

FEATURES

- High power gain
- · Easy power control
- Excellent ruggedness
- Source on mounting base eliminates DC isolators, reducing common mode inductance.

APPLICATIONS

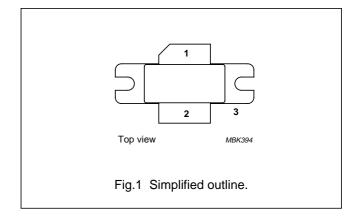
 L-band radar applications in the 1200 to 1400 MHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT502A) with a ceramic cap. The common source is connected to the flange.

PINNING - SOT502A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange



QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	I _{DQ} (mA)	P _L (W)	G _p (dB)	η _D (%)	pulse droop (dB)	t _r (ns)	t _f (ns)
Pulsed class-AB; $t_p = 1 \text{ ms}; \delta = 10\%$	1200 to 1400	36	150	250	>12	>42	<0.6	<100	<100

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V _{DS}	drain-source voltage		_	75	V
V_{GS}	gate-source voltage		_	±22	V
P _{tot}	total power dissipation	$T_h \le 70 ^{\circ}\text{C}; t_p = 1 \text{ms}; \delta = 10\%$	_	400	W
T _{stg}	storage temperature		-65	150	°C
Tj	junction temperature		_	200	°C

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
Z _{th j-h}	thermal impedance from junction to heatsink	T _h = 25 °C, note 1	0.17	K/W
Z _{th j-h}	thermal impedance from junction to heatsink	$T_h = 25 ^{\circ}C$, note 2	0.32	K/W

Notes

- 1. Thermal resistance is determined under RF operating conditions; $t_p = 100 \mu s$, $\delta = 10\%$.
- 2. Thermal resistance is determined under RF operating conditions; t_p = 1 ms, δ = 10%.

CHARACTERISTICS

T_i = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0; I_D = 3 \text{ mA}$	75	-	_	V
V _{GSth}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 300 mA	4	_	5	V
I _{DSS}	drain-source leakage current	V _{GS} = 0; V _{DS} = 36 V	-	_	1	μΑ
I _{DSX}	on-state drain current	$V_{GS} = V_{GSth} + 9 \text{ V}; V_{DS} = 10 \text{ V}$	45	_	_	Α
I _{GSS}	gate leakage current	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0$	_	_	1	μΑ
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 10 A	_	9	_	S
R _{DSon}	drain-source on-state resistance	V _{GS} = 9 V; I _D = 10 A	_	60	_	mΩ

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25$ °C; $Z_{th\ mb-h} = 0.25$ K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V _{DS} (V)	I _{DQ} (mA)	P _L (W)	G _p (dB)	η _D (%)	pulse droop (dB)	t _r (ns)	t _f (ns)
Pulsed class-AB; $t_p = 1$ ms; $\delta = 10\%$	1200 to 1400	36	150	250	>12	>42	<0.6	<100	<100

Ruggedness in class-AB operation

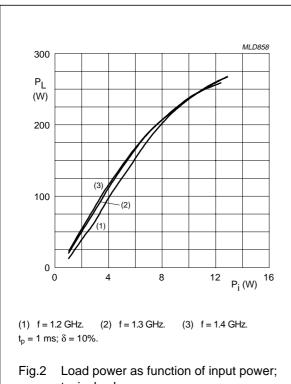
The BLL1214-250 is capable of withstanding a load mismatch corresponding to VSWR = 3: 1 through all phases under the following conditions: $V_{DS} = 36$ V; frequency from 1200 MHz to 1400 MHz at rated load power.

Typical impedance

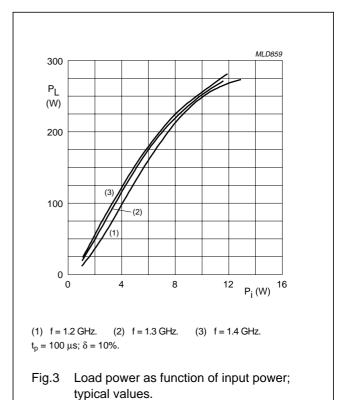
FREQUENCY (GHZ)	Z _S (Ω)	Z _L (Ω)
1.20	1.3 – j 2.8	1.1 – j 0.9
1.25	1.9 – j 2.9	1.0 – j 0.5
1.30	4.6 – j 2.9	0.8 – j 0.2
1.35	5.7 – j 0.3	0.7 – j 0.3
1.40	2.7 – j 1.8	0.6 – j 0.4

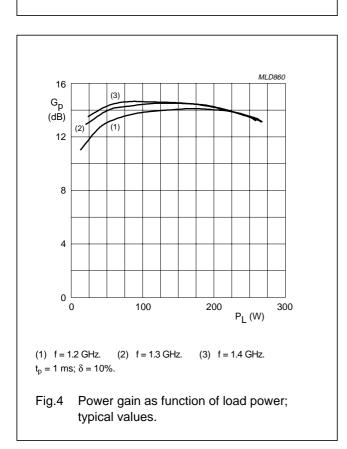
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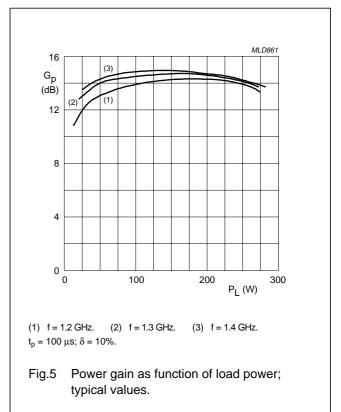
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typical values.



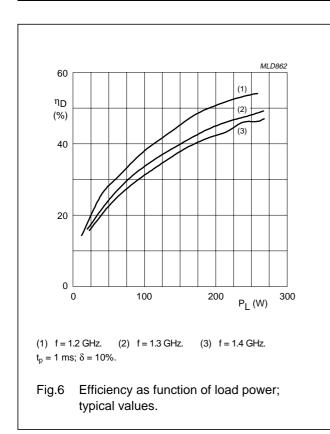




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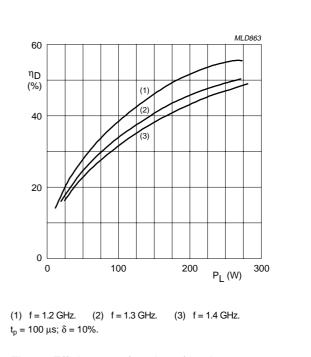
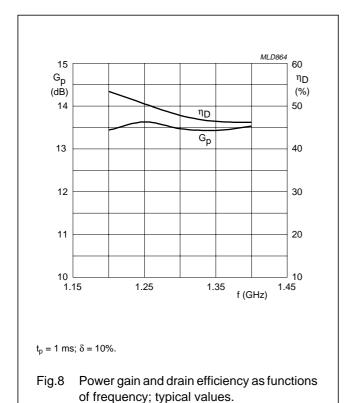
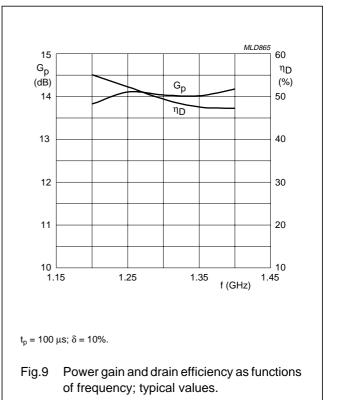


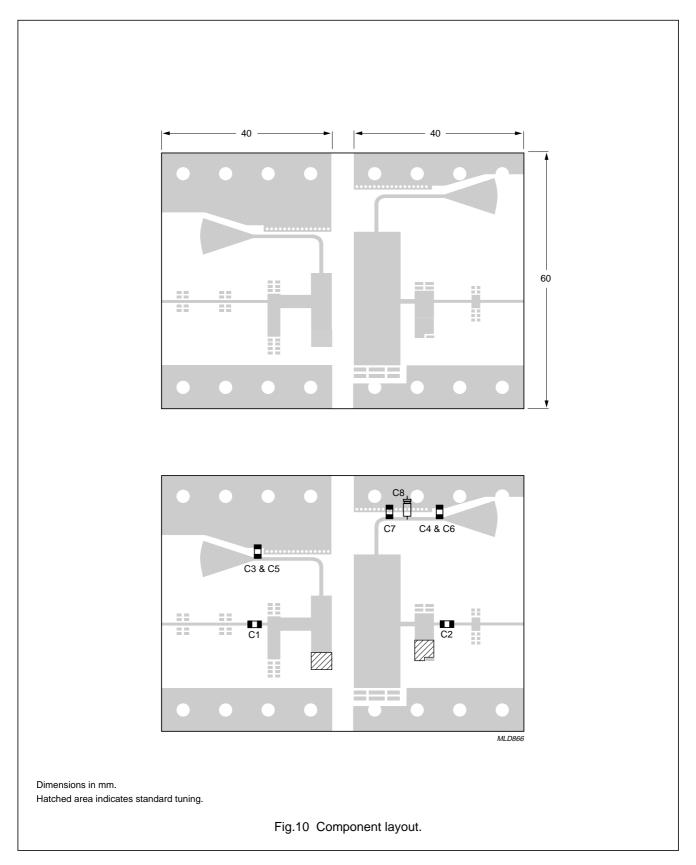
Fig.7 Efficiency as function of load power; typical values.





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List of components (see Fig.10)

COMPONENT	DESCRIPTION	VALUE	CATALOGUE NO.
C1, C3	capacitor	39 pF	ATC100A
C2, C4	capacitor	47 pF	ATC100A
C5, C6	capacitor	20 nF	ATC200B
C7	capacitor	36 pF, 36 pF	ATC200B
C8	electrolytic capacitor	100 μF; 100 V	

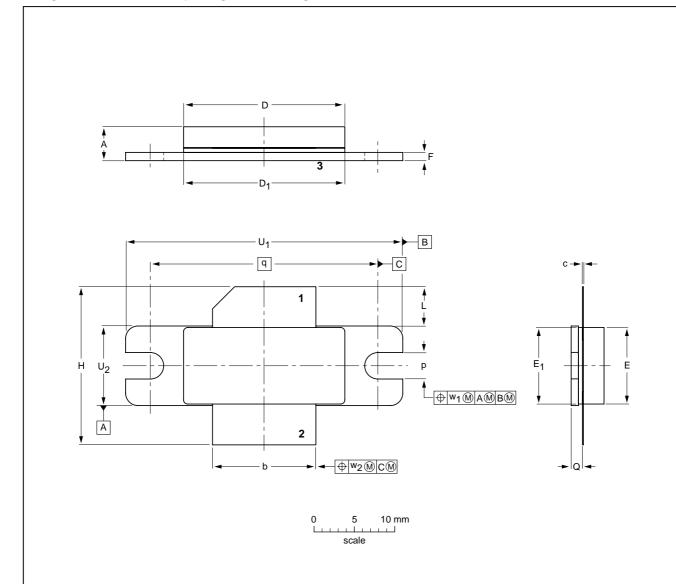
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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT502A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	С	D	D ₁	E	E ₁	F	н	L	р	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.72 3.99	12.83 12.57	0.15 0.08				9.53 9.25	1.14 0.89			3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157										0.133 0.123			1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE		REFER	EUROPEAN	ISSUE DATE		
VERSION	IEC			PROJECTION	ISSUE DATE	
SOT502A						99-10-13 99-12-28

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DATA SHEET STATUS

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Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
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This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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NOTES

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NOTES

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